AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A circuit, comprising:

a power-regulating circuit adapted to respond to a power supply voltage by providing an operating current and an operating voltage to a common node, the power-regulating circuit including,

a current mirror adapted to provide the operating current to the common node; and

a load coupled between the common node and a reference supply and adapted to conduct a first portion of the operating current and, therefrom, establish the operating voltage at the common node, the load including,

a resistive element having a first conductor coupled to the common node; and

a voltage source coupled between a second conductor of the resistive element and the reference supply; [[and]]

an input stage coupled to the common node and adapted to conduct a second portion of the operating current;

an output stage coupled to the common node and adapted to conduct a third portion of the operating current; and

a stabilizer coupled to the common node and adapted to provide a compensation current to the common node to stabilize the operating voltage at the common node in response to differences between a first reference voltage and a feedback voltage indicative of variations at the common node.

Claims 2-5. (Cancelled)

6. (Currently Amended) A circuit adapted to generate constant operational signals from a power supply voltage, comprising:

a current mirror adapted to generate an operating current from the power supply voltage and coupled to supply the operating current to a common node;

a voltage regulator adapted to generate an operating voltage from a first portion

of the operating current and coupled to supply the operating voltage to the common node;

an output stage adapted to conduct a second portion of the operating current to generate an output signal referenced to the operating voltage; [[and]]

an input stage adapted to conduct a third portion of the operating current in response to an input signal received by the circuit; and

a common mode stabilizer adapted to compare the operating voltage to a first reference voltage and further adapted to compensate the operating current to cancel variations in the operating voltage at the common node.

7. (Original) The circuit according to Claim 6, wherein the current mirror comprises:

a first current source coupled to receive a second reference voltage and adapted to provide a bias current in response to the second reference voltage;

a first voltage source coupled to receive the bias current and adapted to provide a bias voltage in response to the bias current; and

a second current source coupled to receive the bias voltage and adapted to supply the operating current in ratio proportion to the bias current.

8. (Original) The circuit according to Claim 6, wherein the voltage regulator comprises:

a resistive element having a first conductor coupled to receive the first portion of the operating current at the common node and having a second conductor coupled to provide the first portion of the operating current; and

a second voltage source coupled to receive the first portion of the operating current and adapted to supply the operating voltage.

9. (Original) The circuit according to Claim 8, wherein the second voltage source includes a current conduction device having a control terminal and a conduction terminal coupled together at the second conductor of the resistive element.

10. (Original) The circuit according to Claim 9, wherein the current conduction device includes a Field Effect Transistor (FET).

11. (Original) The circuit according to Claim 6, wherein the common mode stabilizer comprises:

an error signal generator having a first input coupled to the common node, a second input coupled to receive the first reference voltage, and an output adapted to provide an error signal indicative of a difference between the operating voltage and the first reference voltage; and

a current conduction device having a control terminal coupled to receive the error signal and coupled to provide the compensating current to the common node in response to the error signal.

12. (Original) The circuit according to Claim 11, wherein the error signal generator includes an operational amplifier.

13. (Original) The circuit according to Claim 11, wherein the error signal generator includes an operational transconductance amplifier.

14. (Original) The circuit according to Claim 11, wherein the current conduction device includes a Field Effect Transistor (FET).

15. (Currently Amended) A locally regulated circuit, comprising:

means for generating a constant current signal from a power supply signal;

means for generating a voltage signal from a first portion of the constant current signal;

means for conducting a second portion of the constant current signal to generate an output signal referenced to the voltage signal;

means for conducting a third portion of the constant current signal in response to a received input signal;

means for comparing the voltage signal to a reference signal to generate an

error signal; and

means for compensating the constant current signal in response to the error signal to regulate the voltage signal.

16. (Currently amended) A method of operating a locally regulated circuit, the method comprising:

generating a constant current signal from a power supply signal;

generating a voltage signal from a first portion of the constant current signal;

conducting a second portion of the constant current signal to generate an output signal referenced to the voltage signal;

conducting a third portion of the constant current signal in response to receiving an input signal;

comparing the voltage signal to a reference signal to generate an error signal; and

compensating the constant current signal in response to the error signal to regulate the voltage signal.

17. (Original) The method according to Claim 16, wherein generating the constant current signal comprises:

generating a bias current in response to a reference voltage; and

generating a bias voltage in response to the bias current, wherein the bias voltage induces a magnitude of the constant current signal to be in ratio proportion to the bias current.

18. (Original) The method according to Claim 17, wherein generating the voltage signal comprises:

generating a first reference voltage from the first portion of the constant current signal; and

summing the first reference voltage with a second reference voltage generated by conducting the first portion of the constant current signal through a resistive element.

19. (Original) The method according to Claim 16, wherein comparing the voltage signal to a reference signal includes generating a difference between the voltage signal and the reference signal.

20. (Original) The method according to Claim 19, wherein compensating the constant current signal comprises:

increasing a magnitude of a variable current signal in response to a decreasing magnitude of the error signal; and

decreasing the magnitude of the variable current signal in response to an increasing magnitude of the error signal.

21. (Original) The method according to Claim 20, wherein compensating the constant current signal further comprises summing the constant current signal with the variable current signal to offset variations in the voltage signal.